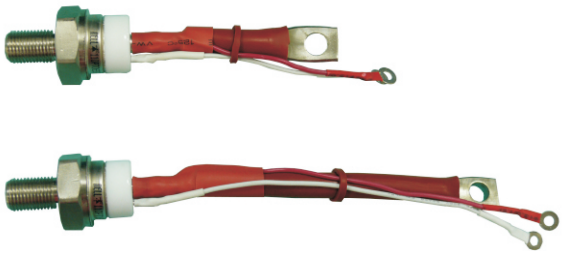
Phase Control Thyristors
(Stud version, 110A)

FEATURES

- High current and high surge capability
- Hermetic ceramic housing
- Planar SCR chips
- Compliant to RoHS
- Designed and qualified for multiple level



TO-209AC (TO-94)

TYPICAL APPLICATIONS

- DC motor control and drives
- Battery chargers
- AC controllers
- Controlled DC power supplies

PRODUCT SUMMARY	
$I_{T(AV)}$	110A

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUE	UNITS
$I_{T(AV)}$	90°C	110	A
$I_{T(RMS)}$	90°C	173	A
I_{TSM}/I_{FSM}	50 Hz	2250	
	60 Hz	2360	
I^2t	50 Hz	25.3	kA^2s
	60 Hz	23.1	
$I^2\sqrt{t}$		253	$kA^2\sqrt{s}$
V_{DRM}/V_{RRM}	Range	400 to 1600	V
t_q	typical	110	μS
T_J	Range	-40 to 150	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 150 °C mA
110PT..S	04	400	500	20
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNIT
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave, 50Hz			110	A
					90	°C
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave, 50Hz, T_C=90°C			173	A
Maximum peak, one-cycle, on-state non-reptitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial $T_J = T_J$ maximum	2250	A
		t = 8.3 ms			2360	
		t = 10 ms	100%V_{RRM} reapplied		1890	
		t = 8.3 ms			1980	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		25.3	kA^2s
		t = 8.3 ms			23.1	
		t = 10 ms	100%V_{RRM} reapplied		17.9	
		t = 8.3 ms			16.3	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			253	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7% x π x $I_{T(AV)}$) < I < π x $I_{T(AV)}$, $T_J = T_J$ maximum			0.80	V
High level value of threshold voltage	$V_{T(TO)2}$	I > π x $I_{T(AV)}$, $T_J = T_J$ maximum			1.05	
Low level value of on-state slope resistance	r_{t1}	(16.7% x π x $I_{T(AV)}$) < I < π x $I_{T(AV)}$, $T_J = T_J$ maximum			2.10	mΩ
High level value of on-state slope resistance	r_{t2}	I > π x $I_{T(AV)}$, $T_J = T_J$ maximum			1.75	
Maximum on-state voltage drop	V_{TM}	I_{TM} = 350A, T_J = 25°C, 180°C conduction			1.6	V
Maximum holding current	I_H	Anode supply = 6V, resistive load T_J = 25°C			150	mA
Maximum latching current	I_L	Anode supply = 6V, resistive load T_J = 25°C			400	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM} I_{DRM}	T_J = 150°C	20	mA
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67% rated V_{DRM}	1000	V/μs

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	Voltage code	UNITS
Typical delay time	t_d	Gate current 1A, dI_g/dt = 1A/μs V_d = 67% V_{DRM}, T_J = 25°C	1	μs
Typical turn-off time	t_q	I_{TM} = 50A, $T_J = T_J$ maximum, dI/dt = -5 A/μs V_R = 50V, dV/dt = 20 V/μs, gate 0V, 25Ω	110	

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES Max.	UNITS
Maximum peak gate power	P_{GM}	$t_p \le 5ms$, $T_J = T_J$ maximum		12		W
Maximum average gate power	$P_{G(AV)}$	f = 50Hz, $T_J = T_J$ maximum		3		W
Maximum peak positive gate current	I_{GM}	$t_p \le 5ms$, $T_J = T_J$ maximum		3		A
Maximum peak positive gate voltage	$+V_{GM}$	$t_p \le 5ms$, $T_J = T_J$ maximum		20		V
Maximum peak negative gate voltage	$-V_{GM}$	$t_p \le 5ms$, $T_J = T_J$ maximum		10		V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = -40°C	Anode supply = 12V, resistive load; R_L = 30Ω	1.60	-	V
		T_J = 25°C		1.0	1.5	V
		T_J = 150°C		0.7	-	V
Maximum required DC gate current to trigger	I_{GT}	T_J = -40°C		140	-	mA
		T_J = 25°C		60	120	mA
		T_J = 150°C		30	-	mA
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, 66.7% V_{DRM} applied		0.25		V
Maximum gate current that will not trigger	I_{GD}	$T_J = T_J$ maximum, 66.7% V_{DRM} applied		10		mA
Maximum rate of rise of turmed-on current	dI/dt	T_J = 25°C, I_{GM} = 1.5A, $t_r \le 0.5$ µs		150		A/µs

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to 150	°C
Maximum junction operating temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.25	°C/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.1	°C/W
Mounting torque, ±10%		Non-lubricated threads	15.5 (137)	N·m (lbf·in)
		Lubricated threads	14 (120)	N·m (lbf·in)
Approximate weight			115	g
			4.06	oz.
Case style		See dimensions (at the end of datasheet)	TO-209AC (TO-94)	

ΔRthJC CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDUCTIONS	UNITS
180°	0.043	0.031	$T_J = T_J$ maximum	K/W
120°	0.052	0.053		
90°	0.066	0.071		
60°	0.096	0.101		
30°	0.167	0.169		

Note

• The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

ORDERING INFORMATION TABLE

Device code

110	PT	16	S	M
①	②	③	④	⑤

1 - Maximum average on-state current, $I_{T(AV)}$
2 - For phase control thyristors
3 - Voltage code, V_{DRM}/V_{RRM} = code x 100
4 - Stud version
5 - None for standard device, ½" - 20UNF
"M" for metric device, M12 x 1.5
"S" for short flexible lead

Fig.1 Current ratings characteristics

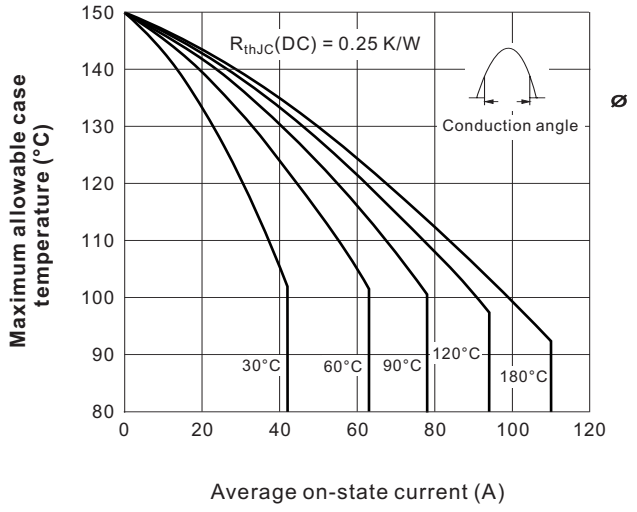


Fig.2 Current ratings characteristics

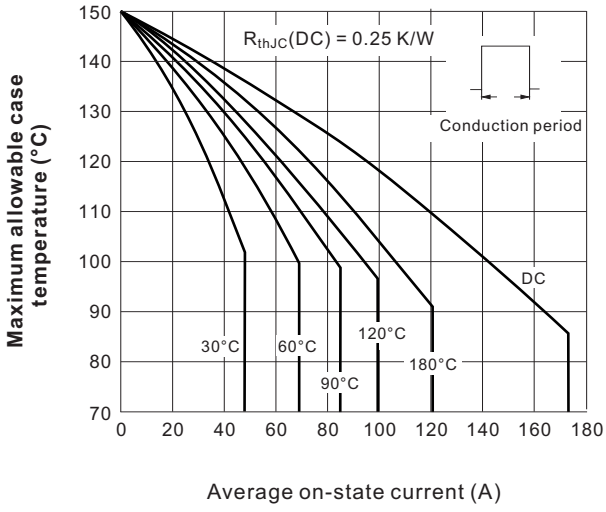
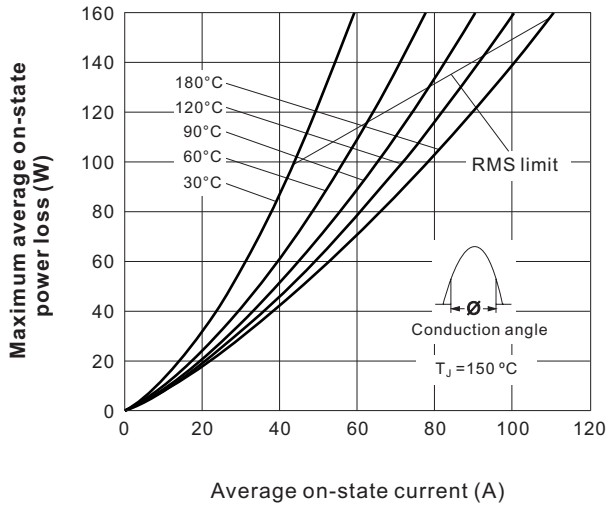


Fig.3 On-State power loss characteristics



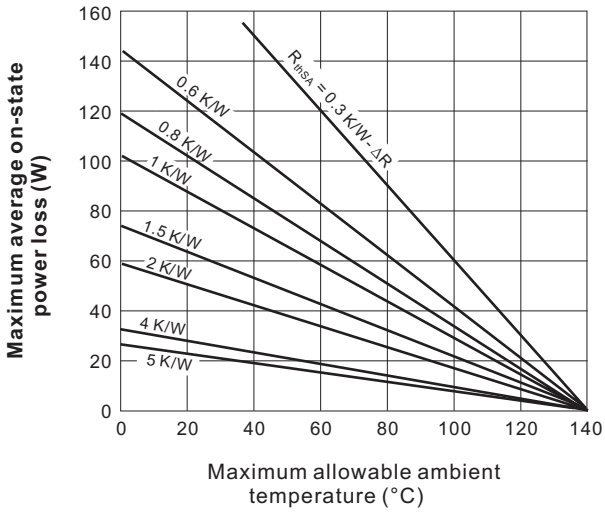
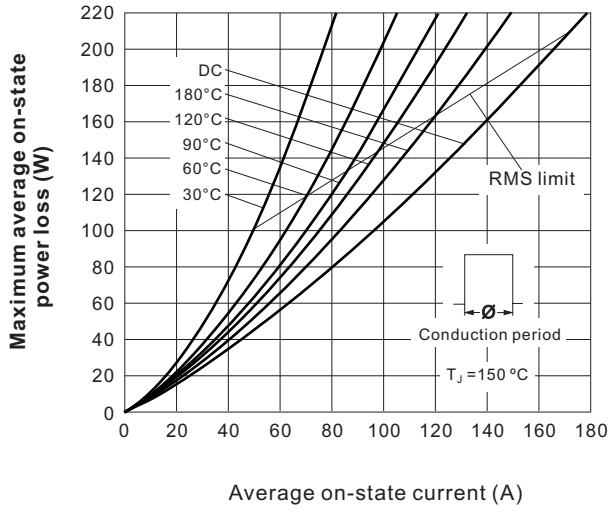


Fig.4 On-State power loss characteristics



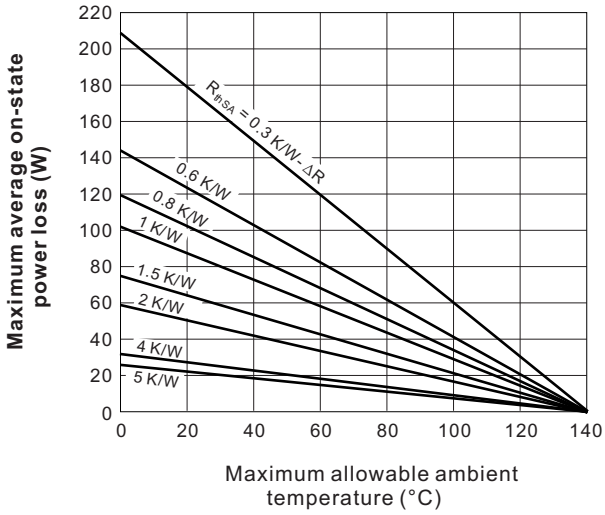


Fig.5 Maximum non-repetitive surge current

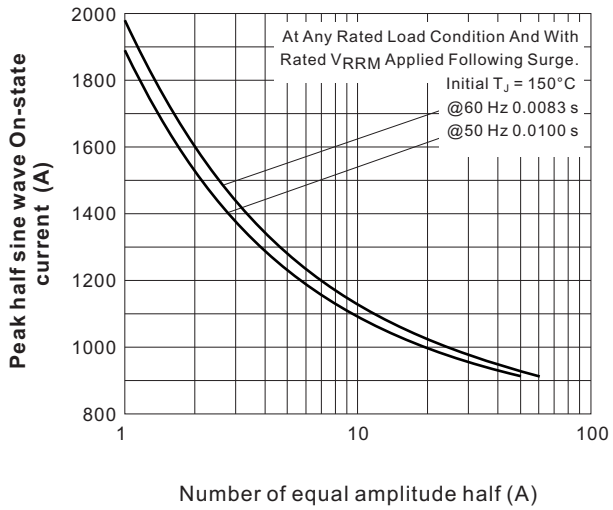


Fig.6 Maximum non-repetitive surge current

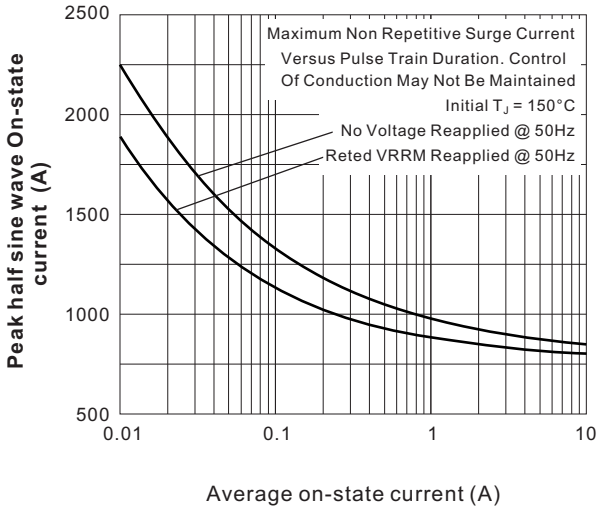


Fig.7 On-state voltage drop characteristics

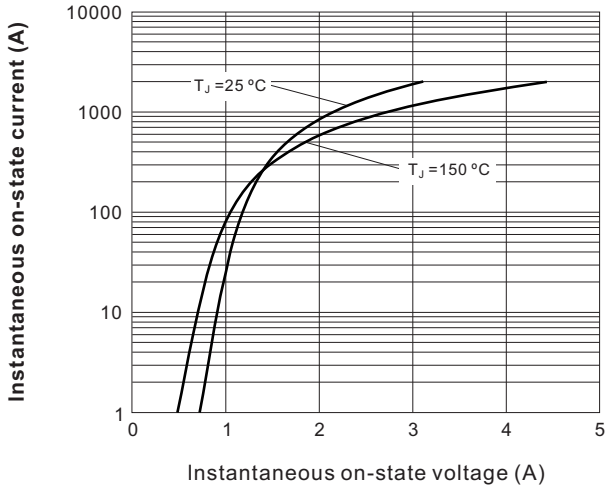


Fig.8 Thermal Impedance Z_{thJC} characteristic

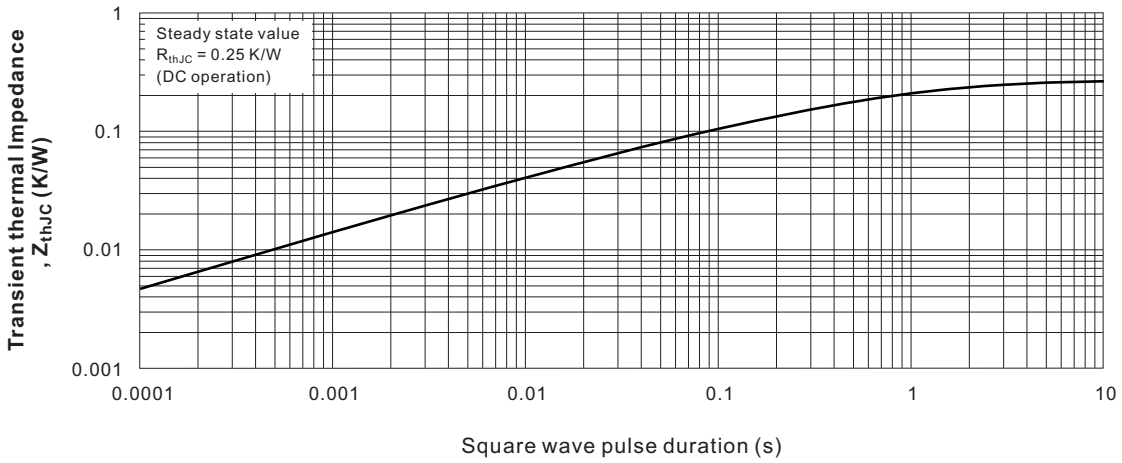
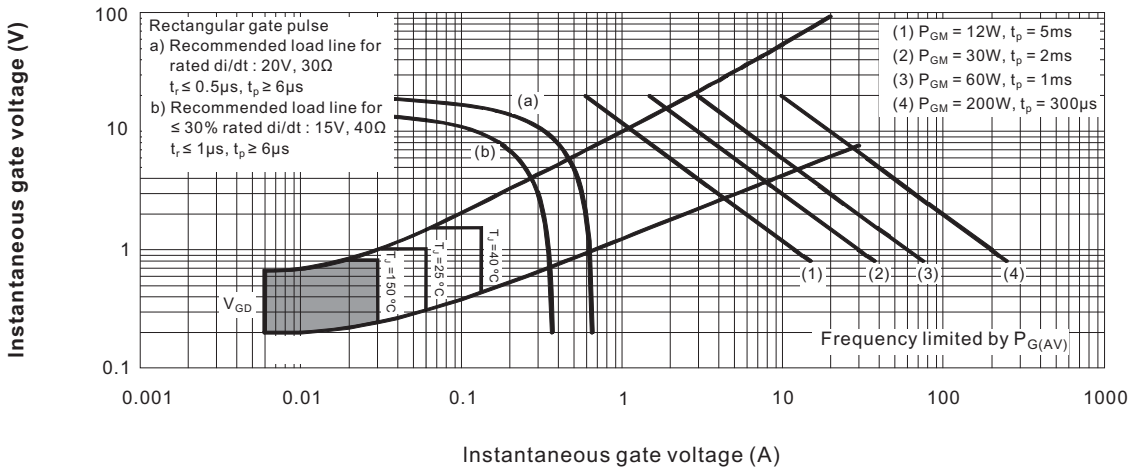
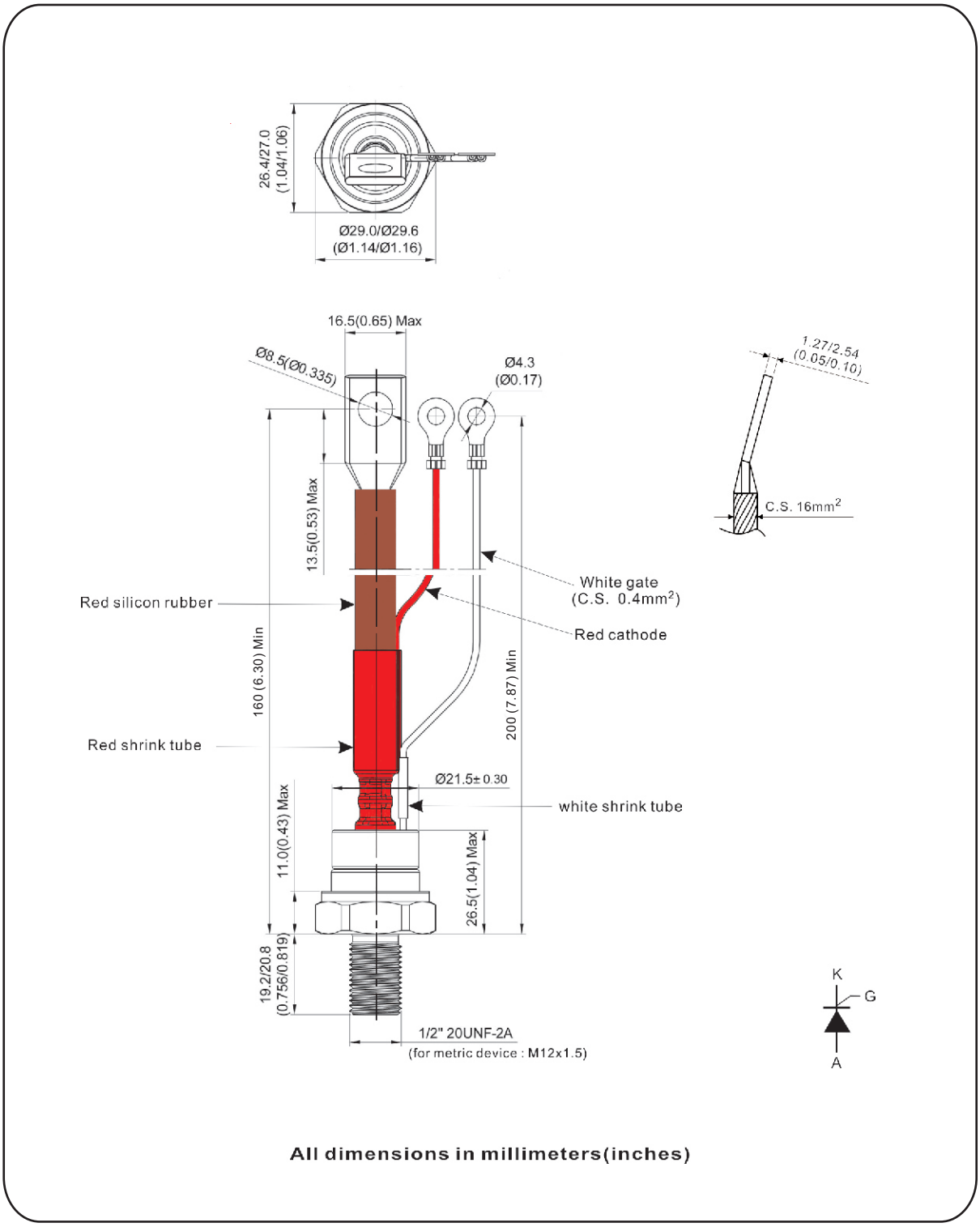


Fig.9 Gate characteristics

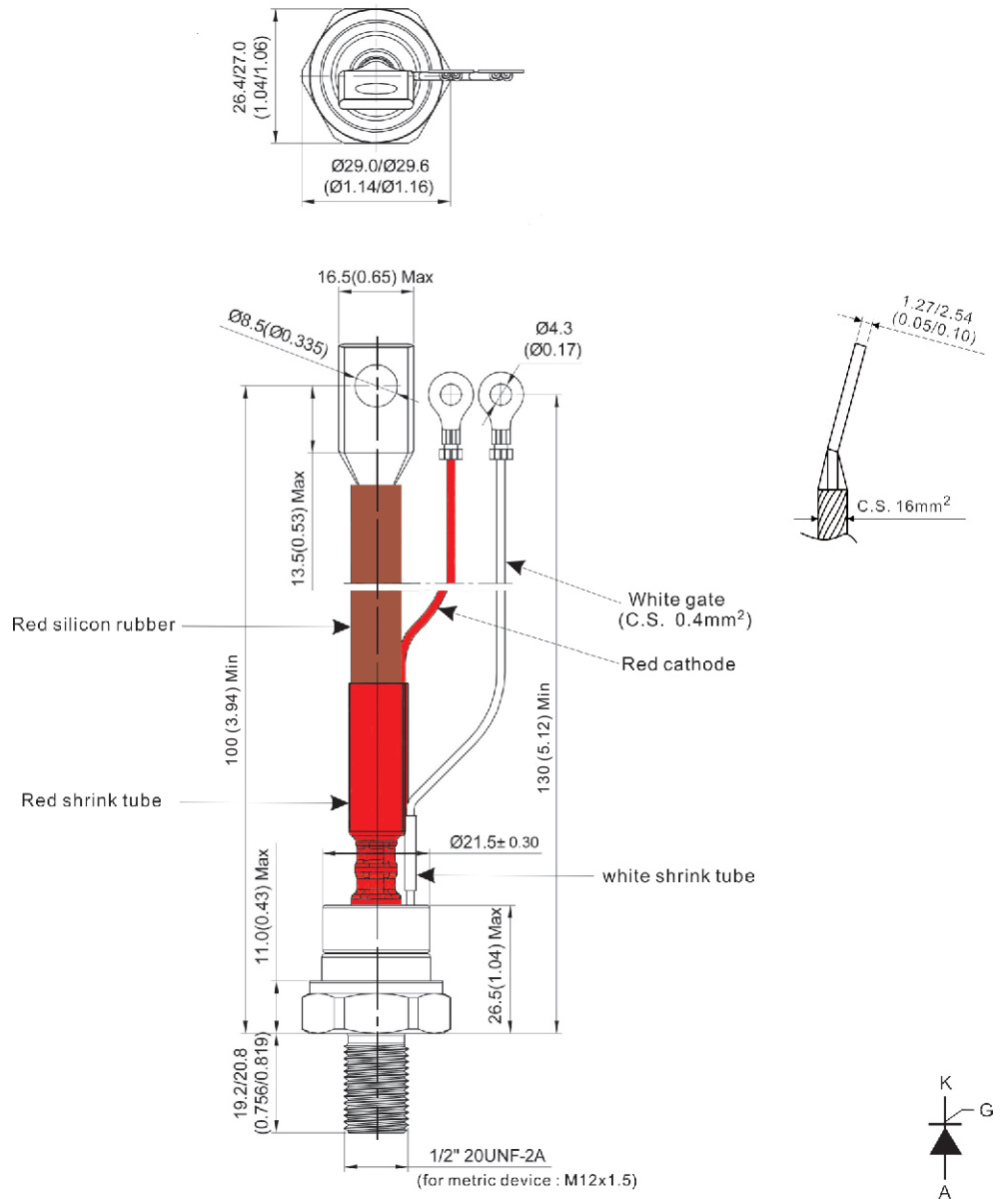


Ceramic Housing



All dimensions in millimeters(inches)

Ceramic housing (for short flexible lead)



All dimensions in millimeters(inches)